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Application Number

			Application Number	10/7/3	132		
INFORMATION DISCLOSURE			Filing Date	Herewith.	122/2004		
STATEMENT BY APPLICANT			First Named Inventor	Peter John McElheny	1/2 /2 (1/2 		
			Art Unit	2825			
(Use as many sheets as necessary)			Examiner Name	PHALLAK	A KIK		
Sheet	1	of 1	Attorney Docket Number	A1167_		ブ	<u> </u>
NON PATENT LITERATURE DOCUMENTS							
Examiner Initials*	Cite No.¹	Include name of the author (in CAPITAL LETTERS), title of the erticle (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.					
P		RAFIK S. GUINDI ET AL., "Design Techniques for Gate-Leakage Reduction in CMOS Circuits," 2003 IEEE pp. 61-65, 24 March 3003,					
(P)		The second secon					2.1-68.
(P)		"Part II Leakage Reduction Techniques", ICCAD 2002 Tutorial; pp 1-50.					. '
Ø)		AFSHIN ABDOLLAHI ET AL., "Runtime Mechanisms for Leakage Current Reduction in CMOS VSLI Circuits", ISLPED' 02, August 12-14, 2002,					
P		JAMES KAO ET AL. "Transistor Sizing Issues and Tool for Multi-Threshold CMOS Technology," DAC 97, Anaheim, CA (c) 1997,					
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P		B. NIKOLIC, "Advanced Digital Circuits" EE241 Lecture Notes, Spring 2002					
B		FEI LI ET AL. "Maximum Current Estimation Considering Power Gating" http://eda.ece.wisc.edu (undated) ; pf < (- 16, University of					
		Wisconsin-Madis	sv.		81		
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